GigaDevice Semiconductor Inc.

GD32F350xx
ARM® Cortex®-M4 32-bit MCU

Datasheet

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1 General description

The GD32F350xx device belongs to the value line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the ARM® Cortex®-M4 RISC core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Cortex®-M4 core features implements a full set of DSP instructions to address digital signal control markets that demand an efficient, easy-to-use blend of control and signal processing capabilities. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32F350xx device incorporates the ARM® Cortex®-M4 32-bit processor core operating at 108 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 128 KB on-chip Flash memory and up to 16 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, one 12-bit DAC and two comparators, up to five general-purpose 16-bit timers, a general-purpose 32-bit timer, a basic timer, a PWM advanced-control timer, as well as standard and advanced communication interfaces: up to two SPIs, two I^2Cs, two USARTs, a I^2S, a HDMI-CEC, a TSI and an USB 2.0 OTG.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F350xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

2 Device overview

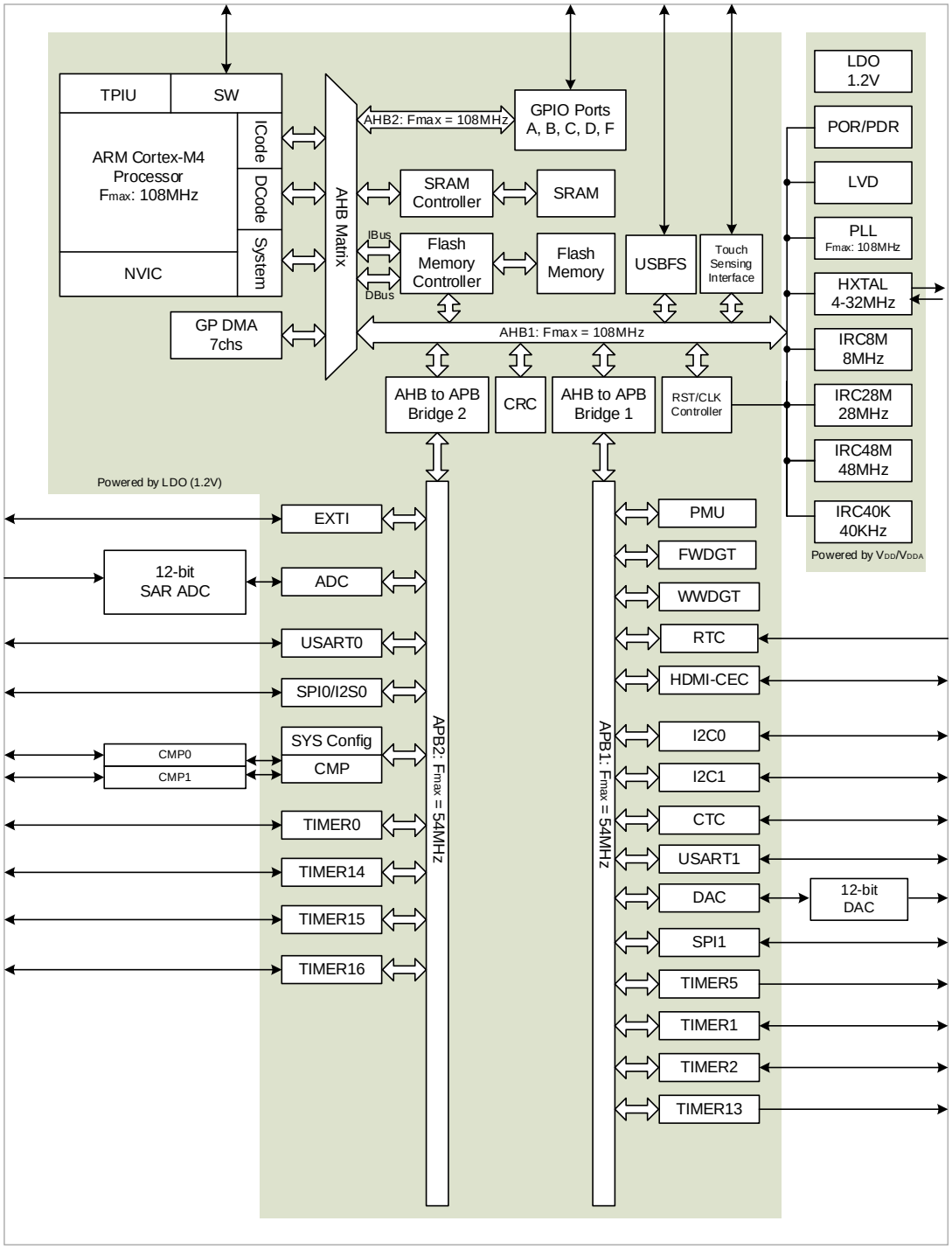
2.1 Device information

Table 1. GD32F350xx devices features and peripheral list

Part Number		GD32F350xx													
		G4	G6	G8	K4	K6	K8	C4	C6	C8	CB	R4	R6	R8	RB
Flash	Code Area (KB)	16	32	64	16	32	64	16	32	64	64	16	32	64	64
	Data Area (KB)	0	0	0	0	0	0	0	0	0	64	0	0	0	64
	Total (KB)	16	32	64	16	32	64	16	32	64	128	16	32	64	128
SRAM (KB)		4	6	8	4	6	8	4	6	8	16	4	8	16	16
Timers	32-bit GP	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	16-bit GP	5	5	5	5	5	5	5	5	5	5	5	5	5	5
	16-bit Adv.	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	16-bit Basic	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	SysTick	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Connectivity	USART	1	2	2	1	2	2	1	2	2	2	1	2	2	2
	I2C	1	1	2	1	1	2	1	1	2	2	1	1	2	2
	SPI/I2S	1/1	1/1	2/1	1/1	1/1	2/1	1/1	1/1	2/1	2/1	1	1	2/1	2/1
	USB 2.0 OTG	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	HDMI CEC	1	1	1	1	1	1	1	1	1	1	1	1	1	1
GPIO		24	24	24	27	27	27	39	39	39	39	55	55	55	55
Capacitive Touch Channels		14	14	14	14	14	14	17	17	17	17	18	18	18	18
Analog Comparator		2	2	2	2	2	2	2	2	2	2	2	2	2	2
EXTI		16	16	16	16	16	16	16	16	16	16	16	16	16	16
ADC	Units	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Channels (Ext.)	10	10	10	10	10	10	10	10	10	10	16	16	16	16
	Channels (Int.)	3	3	3	3	3	3	3	3	3	3	3	3	3	3
DAC		1	1	1	1	1	1	1	1	1	1	1	1	1	1
Package		QFN28			QFN32			LQFP48				LQFP64			

2.2 Block diagram

Figure 1. GD32F350xx block diagram



2.3 Pinouts and pin assignment

Figure 2. GD32F350Rx LQFP64 pinouts

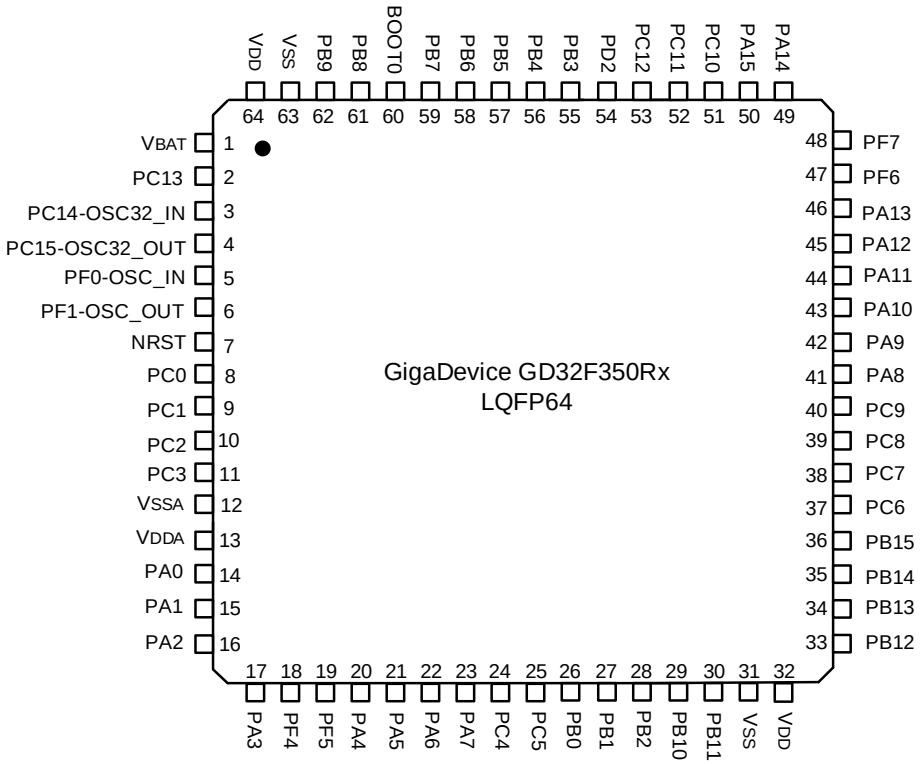


Figure 3. GD32F350Cx LQFP48 pinouts

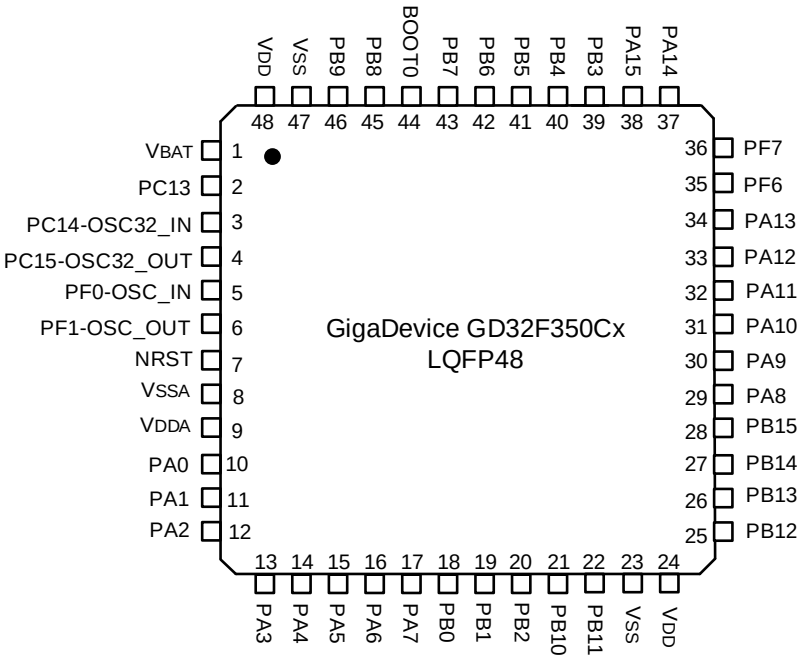


Figure 4. GD32F350Kx QFN32 pinouts

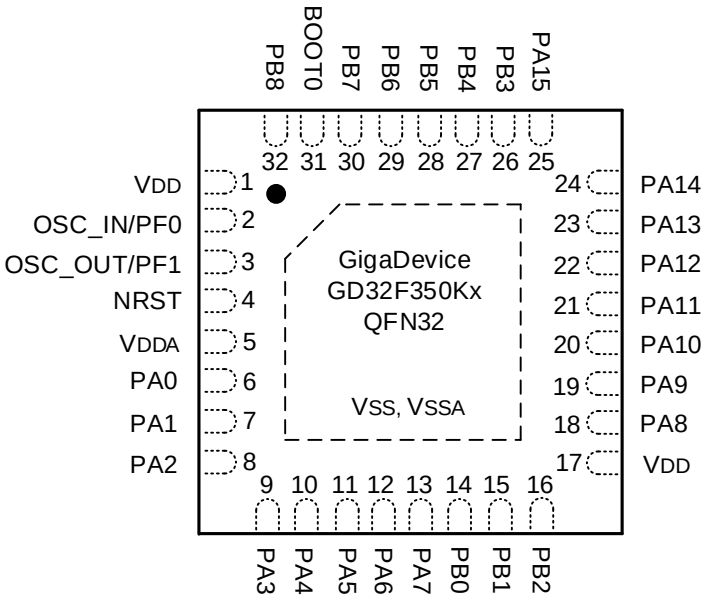
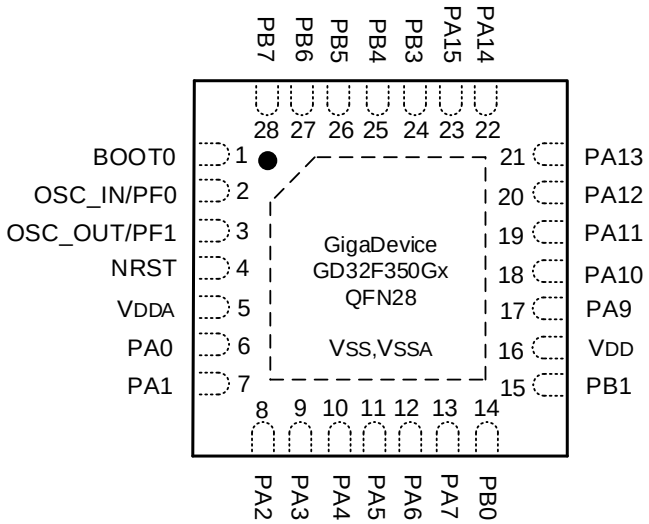


Figure 5. GD32F350Gx QFN28 pinouts



2.4 Memory map

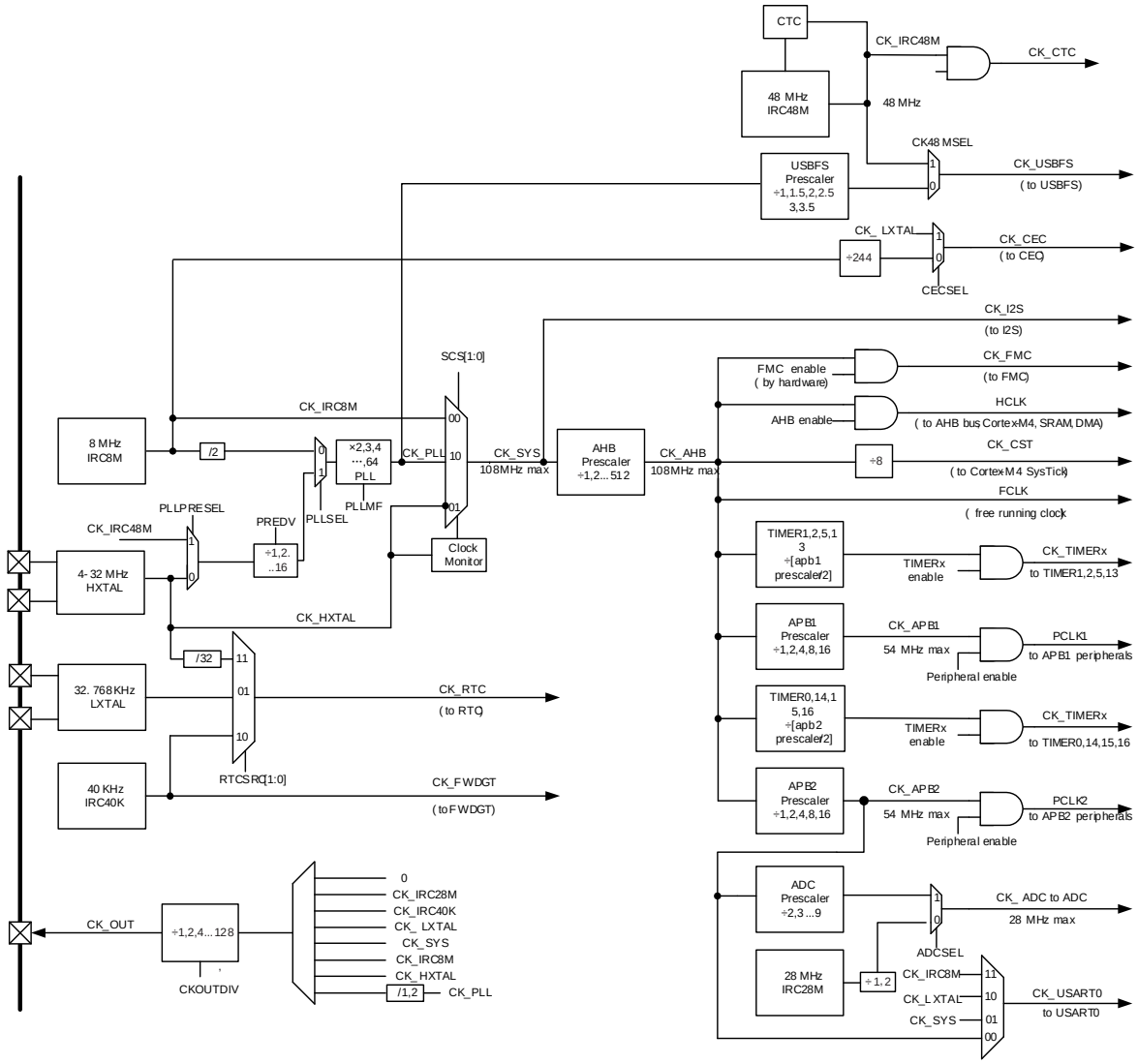
Figure 6. GD32F350xx memory map

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
External Device		0xA000 0000 - 0xDFFF FFFF	Reserved
External RAM		0x6000 0000 - 0x9FFF FFFF	Reserved
Peripherals	AHB1	0x5004 0000 - 0x5FFF FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	USBFS
	AHB2	0x4800 1800 - 0x4FFF FFFF	Reserved
		0x4800 1400 - 0x4800 17FF	GPIOF
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	GPIOD
		0x4800 0800 - 0x4800 0BFF	GPIOC
		0x4800 0400 - 0x4800 07FF	GPIOB
		0x4800 0000 - 0x4800 03FF	GPIOA
	AHB1	0x4002 4400 - 0x47FF FFFF	Reserved
		0x4002 4000 - 0x4002 43FF	TSI
		0x4002 3400 - 0x4002 3FFF	Reserved
		0x4002 3000 - 0x4002 33FF	CRC
		0x4002 2400 - 0x4002 2FFF	Reserved
		0x4002 2000 - 0x4002 23FF	FMC
		0x4002 1400 - 0x4002 1FFF	Reserved
		0x4002 1000 - 0x4002 13FF	RCU
		0x4002 0400 - 0x4002 0FFF	Reserved
		0x4002 0000 - 0x4002 03FF	DMA
	APB2	0x4001 8000 - 0x4001 FFFF	Reserved
		0x4001 5C00 - 0x4001 7FFF	Reserved
		0x4001 4C00 - 0x4001 5BFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	USART0
		0x4001 3400 - 0x4001 37FF	Reserved
		0x4001 3000 - 0x4001 33FF	SPI0/I2S0
		0x4001 2C00 - 0x4001 2FFF	TIMER0
		0x4001 2800 - 0x4001 2BFF	Reserved
		0x4001 2400 - 0x4001 27FF	ADC
		0x4001 0800 - 0x4001 23FF	Reserved
		0x4001 0400 - 0x4001 07FF	EXTI

Pre-defined Regions	Bus	ADDRESS	Peripherals
		0x4001 0000 - 0x4001 03FF	SYSCFG + CMP
	APB1	0x4000 CC00 - 0x4000 FFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	CTC
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	Reserved
		0x4000 8000 - 0x4000 BFFF	Reserved
		0x4000 7C00 - 0x4000 7FFF	Reserved
		0x4000 7800 - 0x4000 7BFF	CEC
		0x4000 7400 - 0x4000 77FF	DAC
		0x4000 7000 - 0x4000 73FF	PMU
		0x4000 6400 - 0x4000 6FFF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	Reserved
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 4800 - 0x4000 53FF	Reserved
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	Reserved
		0x4000 3C00 - 0x4000 3FFF	Reserved
		0x4000 3800 - 0x4000 3BFF	SPI1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	FWDGT
		0x4000 2C00 - 0x4000 2FFF	WWDGT
		0x4000 2800 - 0x4000 2BFF	RTC
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	TIMER13
		0x4000 1400 - 0x4000 1FFF	Reserved
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0800 - 0x4000 0FFF	Reserved
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x2000 5000 - 0x3FFF FFFF	Reserved
		0x2000 0000 - 0x2000 4FFF	SRAM
Code		0x1FFF FC00 - 0x1FFF FFFF	Reserved
		0x1FFF F800 - 0x1FFF FBFF	Option bytes
		0x1FFF EC00 - 0x1FFF F7FF	System memory
		0x0810 0000 - 0x1FFF EBFF	Reserved
		0x0800 0000 - 0x080F FFFF	Main Flash memory
		0x0010 0000 - 0x07FF FFFF	Reserved
		0x0000 0000 - 0x000F FFFF	Aliased to Flash or system memory

2.5 Clock tree

Figure 7. GD32F350xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC8M: Internal 8M RC oscillators

IRC48M: Internal 48M RC oscillators

IRC32K: Internal 32K RC oscillator

2.6 Pin definitions

Table 2. GD32F350xx pin definitions

Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	LQFP64	LQFP48	QFN32	QFN28			
V_{BAT}	1	1	-	-	P		Default: V_{BAT}
PC13-TAMPER-RTC	2	2	-	-	I/O		Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1
PC14-OSC32IN	3	3	-	-	I/O		Default: PC14 Additional: OSC32IN
PC15-OSC32OUT	4	4	-	-	I/O		Default: PC15 Additional: OSC32OUT
PF0-OSCIN	5	5	2	2	I/O	5VT	Default: PF0 Alternate: CTC_SYNC Additional: OSCIN
PF1-OSCOUT	6	6	3	3	I/O	5VT	Default: PF1 Additional: OSCOUT
NRST	7	7	4	4	I/O		Default: NRST
PC0	8	-	-	-	I/O		Default: PC0 Alternate: EVENTOUT Additional: ADC_IN10
PC1	9	-	-	-	I/O		Default: PC1 Alternate: EVENTOUT Additional: ADC_IN11
PC2	10	-	-	-	I/O		Default: PC2 Alternate: EVENTOUT Additional: ADC_IN12
PC3	11	-	-	-	I/O		Default: PC3 Alternate: EVENTOUT Additional: ADC_IN13
V_{SSA}	12	8	0	0	P		Default: V_{SSA}
V_{DDA}	13	9	5	5	P		Default: V_{DDA}
PA0-WKUP	14	10	6	6	I/O		Default: PA0 Alternate: USART0_CTS(3), USART1_CTS(4), TIMER1_CH0, TIMER1_ETI, CMP0_OUT, TSI_G0_IO0, I2C1_SCL Additional: ADC_IN0, CMP0_IM6, RTC_TAMP1, WKUP0
PA1	15	11	7	7	I/O		Default: PA1 Alternate: USART0_RTS(3), USART1_RTS(4), TIMER1_CH1, TSI_G0_IO1, I2C1_SDA, EVENTOUT Additional: ADC_IN1, CMP0_IP

Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	LQFP64	LQFP48	QFN32	QFN28			
PA2	16	12	8	8	I/O		Default: PA2 Alternate: USART0_TX(3), USART1_TX(4), TIMER1_CH2, TIMER14_CH0 , CMP1_OUT,TSI_G0_IO2 Additional: ADC_IN2, CMP1_IM6
PA3	17	13	9	9	I/O		Default: PA3 Alternate: USART0_RX(3), USART1_RX(4), TIMER1_CH3, TIMER14_CH1, TSI_G0_IO3 Additional: ADC_IN3, CMP1_IP
PF4	18	-	-	-	I/O	5VT	Default: PF4 Alternate: EVENTOUT
PF5	19	-	-	-	I/O	5VT	Default: PF5 Alternate: EVENTOUT
PA4	20	14	10	10	I/O		Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_CK(3), USART1_CK(4), TIMER13_CH0, TSI_G1_IO0, SPI1_NSS Additional: ADC_IN4, CMP0_IM4, CMP1_IM4, DAC0_OUT
PA5	21	15	11	11	I/O		Default: PA5 Alternate: SPI0_SCK, I2S0_CK, CEC, TIMER1_CH0, TIMER1_ETI, TSI_G1_IO1 Additional: ADC_IN5, CMP0_IM5, CMP1_IM5
PA6	22	16	12	12	I/O		Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BKIN, TIMER15_CH0, CMP0_OUT, TSI_G1_IO2, EVENTOUT Additional: ADC_IN6
PA7	23	17	13	13	I/O		Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, CMP1_OUT, TSI_G1_IO3, EVENTOUT Additional: ADC_IN7
PC4	24	-	-	-	I/O		Default: PC4 Alternate: EVENTOUT Additional: ADC_IN14
PC5	25	-	-	-	I/O		Default: PC5 Alternate: TSI_G2_IO0 Additional: ADC_IN15, WKUP4
PB0	26	18	14	14	I/O		Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, TSI_G2_IO1, USART1_RX, EVENTOUT Additional: ADC_IN8
PB1	27	19	15	15	I/O		Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, TSI_G2_IO2, SPI1_SCK Additional: ADC_IN9

Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	LQFP64	LQFP48	QFN32	QFN28			
PB2	28	20	16	-	I/O	5VT	Default: PB2 Alternate: TSI_G2_IO3
PB10	29	21	-	-	I/O	5VT	Default: PB10 Alternate: I2C0_SCL(3),I2C1_SCL(4), CEC, TIMER1_CH2, TSITG, SPI1_IO2
PB11	30	22	-	-	I/O	5VT	Default: PB11 Alternate: I2C0_SDA(3),I2C1_SDA(4), TIMER1_CH3, TSI_G5_IO0, EVENTOUT, SPI1_IO3
V_{SS}	31	23	-	-	P		Default: V_{SS}
V_{DD}	32	24	17	16	P		Default: V_{DD}
PB12	33	25	-	-	I/O	5VT	Default: PB12 Alternate: SPI0_NSS(3), SPI1_NSS(4), TIMER0_BKIN, TSI_G5_IO1, I2C1_SMBA, EVENTOUT
PB13	34	26	-	-	I/O	5VT	Default: PB13 Alternate: SPI0_SCK(3), SPI1_SCK(4), TIMER0_CH0_ON, TSI_G5_IO2
PB14	35	27	-	-	I/O	5VT	Default: PB14 Alternate: SPI0_MISO(3), SPI1_MISO(4), TIMER0_CH1_ON, TIMER14_CH0, TSI_G5_IO3
PB15	36	28	-	-	I/O	5VT	Default: PB15 Alternate: SPI0_MOSI(3), SPI1_MOSI(4), TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN, WKUP6
PC6	37	-	-	-	I/O	5VT	Default: PC6 Alternate: TIMER2_CH0, I2S0_MCK
PC7	38	-	-	-	I/O	5VT	Default: PC7 Alternate: TIMER2_CH1
PC8	39	-	-	-	I/O	5VT	Default: PC8 Alternate: TIMER2_CH2
PC9	40	-	-	-	I/O	5VT	Default: PC9 Alternate: TIMER2_CH3
PA8	41	29	18	-	I/O	5VT	Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT, USART1_TX, EVENTOUT,USBFS_SOF,CTC_SYNC
PA9	42	30	19	17	I/O	5VT	Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BKIN, TSI_G3_IO0, I2C0_SCL,USBFS_VBUS
PA10	43	31	20	18	I/O	5VT	Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BKIN, TSI_G3_IO1, I2C0_SDA, USBFS_ID
PA11	44	32	21	19	I/O	5VT	Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, CMP0_OUT, TSI_G3_IO2, EVENTOUT, SPI1_IO2

Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	LQFP64	LQFP48	QFN32	QFN28			
							Additional: USBFS_DM
PA12	45	33	22	20	I/O	5VT	Default: PA12 Alternate: USART0_RTS, TIMER0_ETI, CMP1_OUT, TSI_G3_IO3, EVENTOUT, SPI1_IO3 Additional: USBFS_DP
PA13	46	34	23	21	I/O	5VT	Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO
PF6	47	35	-	-	I/O	5VT	Default: PF6 Alternate: I2C0_SCL(3), I2C1_SCL(4)
PF7	48	36	-	-	I/O	5VT	Default: PF7 Alternate: I2C0_SDA(3), I2C1_SDA(4)
PA14	49	37	24	22	I/O	5VT	Default: PA14 Alternate: USART0_TX(3), USART1_TX(4), SWCLK, SPI1_MOSI
PA15	50	38	25	23	I/O	5VT	Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX(3), USART1_RX(4), TIMER1_CH0, TIMER1_ETI, SPI1_NSS, EVENTOUT
PC10	51	-	-	-	I/O	5VT	Default: PC10
PC11	52	-	-	-	I/O	5VT	Default: PC11
PC12	53	-	-	-	I/O	5VT	Default: PC12
PD2	54	-	-	-	I/O	5VT	Default: PD2 Alternate: TIMER2_ETI
PB3	55	39	26	24	I/O	5VT	Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER1_CH1, TSI_G4_IO0, EVENTOUT
PB4	56	40	27	25	I/O	5VT	Default: PB4 Alternate: SPI0_MISO,I2S0_MCK, TIMER2_CH0, TSI_G4_IO1, EVENTOUT
PB5	57	41	28	26	I/O	5VT	Default: PB5 Alternate: SPI0_MOSI,I2S0_SD, I2C0_SMBA, TIMER15_BKIN, TIMER2_CH1 Additional:WKUP5
PB6	58	42	29	27	I/O	5VT	Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON, TSI_G4_IO2
PB7	59	43	30	28	I/O	5VT	Default: PB7 Alternate:I2C0_SDA,USART0_RX,TIMER16_CH0_ON,TSI_G4_IO3
BOOT0	60	44	31	1	I		Default: BOOT0
PB8	61	45	32	-	I/O	5VT	Default: PB8 Alternate: I2C0_SCL, CEC, TIMER15_CH0, TSITG
PB9	62	46	-	-	I/O	5VT	Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT, I2S0_MCK
V_{SS}	63	47	0	0	P		Default: V_{SS}

Pin Name	Pins				Pin Type(1)	I/O(2) Level	Functions description
	LQFP64	LQFP48	QFN32	QFN28			
V_{DD}	64	48	1	-	P		Default: V_{DD}

Notes:

1. Type: I = input, O = output, P = power.
2. I/O Level: 5VT = 5 V tolerant.
3. This feature is available on GD32F350x4 devices only.
4. This feature is available on GD32F350x8 and GD32F350x6 devices only.

Table 3. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART0_CTS(1) USART1_CTS(2)	TIMER1_CH0,TIMER1_ ETI	TSI_G0_IO0	I2C1_SCL			CMP0_OUT
PA1	EVENTOUT	USART0_RTS(1) USART1_RTS(2)	TIMER1_CH1	TSI_G0_IO1	I2C1_SDA			
PA2	TIMER14_CH0	USART0_TX(1) USART1_TX(2)	TIMER1_CH2	TSI_G0_IO2				CMP1_OUT
PA3	TIMER14_CH1	USART0_RX(1) USART1_RX(2)	TIMER1_CH3	TSI_G0_IO3				
PA4	SPI0_NSS/ I2S0_WS	USART0_CK(1) USART1_CK(2)		TSI_G1_IO0	TIMER13_CH0		SPI1_NSS	
PA5	SPI0_SCK/ I2S0_CK	CEC	TIMER1_CH0, TIMER1_ ETI	TSI_G1_IO1				
PA6	SPI0_MISO/ I2S0_MCK	TIMER2_CH0	TIMER0_BKIN	TSI_G1_IO2		TIMER15_CH0	EVENTOUT	CMP0_OUT
PA7	SPI0_MOSI/ I2S0_SD	TIMER2_CH1	TIMER0_CH0_ON	TSI_G1_IO3	TIMER13_CH0	TIMER16_CH0	EVENTOUT	CMP1_OUT
PA8	CK_OUT	USART0_CK	TIMER0_CH0	EVENTOUT	USART1_TX	USBFS_SOF	CTC_SYNC	
PA9	TIMER14_BKIN	USART0_TX	TIMER0_CH1	TSI_G3_IO0	I2C0_SCL	USBFS_VBUS		
PA10	TIMER16_BKIN	USART0_RX	TIMER0_CH2	TSI_G3_IO1	I2C0_SDA	USBFS_ID		
PA11	EVENTOUT	USART0_CTS	TIMER0_CH3	TSI_G3_IO2			SPI1_IO2	CMP0_OUT
PA12	EVENTOUT	USART0_RTS	TIMER0_ETI	TSI_G3_IO3			SPI1_IO3	CMP1_OUT
PA13	SWDIO	IFRP_OUT					SPI1_MISO	
PA14	SWCLK	USART0_TX(1) USART1_TX(2)					SPI1_MOSI	
PA15	SPI0_NSS/ I2S0_WS	USART0_RX(1) USART1_RX(2)	TIMER1_CH0, TIMER1_ ETI	EVENTOUT			SPI1_NSS	

1. This feature is available on GD32F350x4 devices only.
2. This feature is available on GD32F350xB, GD32F350x8 and GD32F350x6 devices only.

Table 4. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PB0	EVENTOUT	TIMER2_CH2	TIMER0_CH1_ON	TSI_G2_IO1	USART1_RX		
PB1	TIMER13_CH0	TIMER2_CH3	TIMER0_CH2_ON	TSI_G2_IO2			SPI1_SCK
PB2				TSI_G2_IO3			
PB3	SPI0_SCK / I2S0_CK	EVENTOUT	TIMER1_CH1	TSI_G4_IO0			
PB4	SPI0_MISO / I2S0_MCK	TIMER2_CH0	EVENTOUT	TSI_G4_IO1			
PB5	SPI0_MOSI / I2S0_SD	TIMER2_CH1	TIMER15_BKIN	I2C0_SMBA			
PB6	USART0_TX	I2C0_SCL	TIMER15_CH0_ON	TSI_G4_IO2			
PB7	USART0_RX	I2C0_SDA	TIMER16_CH0_ON	TSI_G4_IO3			
PB8	CEC	I2C0_SCL	TIMER15_CH0	TSITG			
PB9	IFRP_OUT	I2C0_SDA	TIMER16_CH0	EVENTOUT		I2S0_MCK	
PB10	CEC	I2C0_SCL(1), I2C1_SCL(2)	TIMER1_CH2	TSITG			SPI1_IO2
PB11	EVENTOUT	I2C0_SDA(1), I2C1_SDA(2)	TIMER1_CH3	TSI_G5_IO0			SPI1_IO3
PB12	SPI0_NSS(1) SPI1_NSS(2)	EVENTOUT	TIMER0_BKIN	TSI_G5_IO1	I2C1_SMBA		
PB13	SPI0_SCK(1) SPI1_SCK(2)		TIMER0_CH0_ON	TSI_G5_IO2			
PB14	SPI0_MISO(1) SPI1_MISO(2)	TIMER14_CH0	TIMER0_CH1_ON	TSI_G5_IO3			
PB15	SPI0_MOSI(1) SPI1_MOSI(2)	TIMER14_CH1	TIMER0_CH2_ON	TIMER14_CH0_ON			

1. This feature is available on GD32F350x4 devices only.
2. This feature is available on GD32F350xB, GD32F350x8 and GD32F350x6 devices only.

Table 5. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PC0	EVENTOUT						
PC1	EVENTOUT						
PC2	EVENTOUT						
PC3	EVENTOUT						
PC4	EVENTOUT						
PC5	TSI_G2_IO0						
PC6	TIMER2_CH0		I2S0_MCK				
PC7	TIMER2_CH1						
PC8	TIMER2_CH2						
PC9	TIMER2_CH3						
PC10							
PC11							
PC12							
PC13							
PC14							
PC15							

Table 6. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PD0							
PD1							
PD2	TIMER2_ETI						
PD3							
PD4							
PD5							
PD6							
PD7							
PD8							
PD9							
PD10							
PD11							
PD12							
PD13							
PD14							
PD15							

Table 7. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PF0	CTC_SYNC						
PF1							
PF2							
PF3							
PF4	EVENTOUT						
PF5	EVENTOUT						
PF6	I2C0_SCL(1) I2C1_SCL(2)						
PF7	I2C0_SDA(1) I2C1_SDA(2)						
PF8							
PF9							
PF10							
PF11							
PF12							
PF13							
PF14							
PF15							

1. This feature is available on GD32F350x4 devices only.
2. This feature is available on GD32F350xB, GD32F350x8 and GD32F350x6 devices only.

3 Functional description

3.1 ARM® Cortex®-M4 core

The ARM® Cortex®-M4 processor is a high performance embedded processor with DSP instructions which allow efficient signal processing and complex algorithm execution. It brings an efficient, easy-to-use blend of control and signal processing capabilities to meet the digital signal control markets demand. The processor is highly configurable enabling a wide range of implementations from those requiring memory protection and powerful trace technology to cost sensitive devices requiring minimal area, while delivering outstanding computational performance and an advanced system response to interrupts.

32-bit ARM® Cortex®-M4 processor core

- Up to 108 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated DSP instructions
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M4 processor is based on the ARMv7-M architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M4:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2 On-chip memory

- Up to 128 Kbytes of Flash memory
- Up to 16 Kbytes of SRAM with hardware parity checking

The ARM® Cortex®-M4 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 128 Kbytes of inner Flash and 16 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The Figure 7. GD32F350xx memory map shows the memory map of the GD32F350xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3 Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 48 MHz RC oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 108 MHz. See Figure 8 for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 in device mode.

3.5 Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are Sleep mode, Deep-sleep mode, and Standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.
- **Deep-sleep** mode
  In Deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the Deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the Deep-sleep mode, the IRC8M is selected as the system clock.
- **Standby** mode
  In Standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup Registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6 Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 2.6MSPS
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
- Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
- Input voltage range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

One 12-bit 2.6MSPS multi-channel ADCs are integrated in the device. It has a total of 19 multiplexed channels: 16 external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and 1 channel for battery voltage (V_{BAT}). The input voltage range is between V_{SSA} and V_{DDA}. An on-chip hardware oversampling scheme improves performance while off-loading the related computational burden from the CPU. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general-purpose level 0 timers (TMx) and the advanced-control timers (TM0 and TM7) with internal connection. The

temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage in a digital value.

3.7 Digital to analog converter (DAC)

- 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DAC is designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is V_{REF+}.

3.8 DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, I^2Cs, USARTs, DAC and I^2S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9 General-purpose inputs/outputs (GPIOs)

- Up to 55 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 55 general purpose I/O pins (GPIO) in GD32F350xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4-PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull open-drain or analog), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10 Timers and PWM generation

- One 16-bit advanced-control timer (TM0), one 32-bit general-purpose timer (TM1), five 16-bit general-purpose timers (TM2, TM13 ~ TM16), and one 16-bit basic timer (TM5)
- Up to 4 independent channels of PWM, output compare or input capture for each general-purpose timer (GPTM) and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Independent watchdog and window watchdog)

The advanced-control timer (TM0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge- or center-aligned counting modes) and single pulse mode output. If configured as a general-purpose 16-bit timer, it has the same functions as the TMx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM) can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TM1 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TM13 ~ TM16 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TM5, is mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F350xx have two watchdog peripherals, free watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The independent watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It

features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11 Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.
- Calendar with subsecond, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 0.954 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

3.12 Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides two data transfer rates: 100 kHz of standard mode, 400 kHz of the fast mode and 1 MHz of the fast mode plus. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13 Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 30 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14 Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating frequency up to 10.5 MBits/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.15 Inter-IC sound (I2S)

- One I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz, multiplexed with SPI1
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F350xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1. The audio sampling frequency from 8 kHz to 192 kHz is supported with less than 0.5% accuracy error.

3.16 HDMI CEC

- Hardware support Consumer Electronics Control (CEC) protocol (HDMI standard rev1.4)

The CEC protocol provides high-level control functions between the audiovisual products linked with HDMI cables. GD32F350xx contain a HDMI-CEC controller which has an independent clock domain and can wake up the MCU from deep-sleep mode on data reception.

3.17 Universal serial bus on-the-go full-speed (USB OTG FS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal 48 MHz oscillator (IRC48M) support crystal-less operation
- Internal main PLL for USB CLK compliantly
- Internal USB OTG FS PHY support

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers. Transaction formatting is performed by the hardware, including CRC generation and checking. It supports both host and device modes, as well as OTG mode with Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The controller contains a full-speed USB PHY internal. For full-speed or low-speed operation, no more external PHY chip is needed. It supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. The required precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HXTAL crystal oscillator) or by the internal 48 MHz oscillator (IRC48M) in automatic trimming mode that allows crystal-less operation.

3.18 Touch sensing interface (TSI)

- Supports up to 18 external electrodes by the sensing channels distributed over 6 analog I/O groups
- Programmable charging frequency and I/O pins
- Capability to wake up the MCU from power saving modes

Capacitive sensing technology can be used for the detection of a finger (or any conductive object) presence near an electrode. The capacitive variation of the electrode introduced by the finger can be measured by charging and detecting the voltage across the sampling capacitor. GD32F350xx contain a hardware touch sensing interface (TSI) and only requires few external components to operate. The sensing channels are distributed over 6 analog I/O groups including: Group1 (PA0 ~ PA3), Group2 (PA4 ~ PA7), Group3 (PC5, PB0 ~ PB2), Group4 (PA9 ~ PA12), Group5 (PB3, PB4, PB6,PA7) and Group6 (PB11 ~ PB14),

3.19 Comparators (CMP)

- Two fast rail-to-rail low-power comparators with software configurable
- Programmable reference voltage (internal, external I/O or DAC output pin)

Two Comparators (CMP) are implemented within the devices. Both comparators can wake up from deep-sleep mode to generate interrupts and breaks for the timers and also can be combined as a window comparator. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

3.20 Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.21 Package and operation temperature

- LQFP64 (GD32F350Rx), LQFP48 (GD32F350Cx), QFN32 (GD32F350Kx) and QFN28 (GD32F350Gx)
- Operation temperature range: -40°C to +85°C (industrial level)

4 Electrical characteristics

4.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V tolerant pin	V_{SS} - 0.3	V_{DD} + 4.0	V
	Input voltage on other I/O	V_{SS} - 0.3	4.0	V
$\|\Delta V_{DDx}\|$	Variations between different VDD power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	25	mA
T_A	Operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C

4.2 Recommended DC characteristics

Table 9. DC operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	—	2.6	3.3	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	2.6	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.8	—	3.6	V

4.3 Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 10. Power consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD}=V_{DDA}=3.3V, HSE=8MHz, System clock=108 MHz, All peripherals enabled	—	25.12	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=8MHz, System clock =108 MHz, All peripherals disabled	—	19.04	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=8MHz, System clock =84 MHz, All peripherals enabled	-—	19.86	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=8MHz, System Clock =84 MHz, All peripherals disabled	—	15.14	—	mA
	Supply current (Sleep mode)	V_{DD}=V_{DDA}=3.3V, HSE=8MHz, CPU clock off, System clock =108 MHz, All peripherals enabled	—	13.22	—	mA
		V_{DD}=V_{DDA}=3.3V, HSE=8MHz, CPU clock off, System clock =108 MHz, All peripherals disabled	—	6.30	—	mA
	Supply current (Deep-Sleep mode)	V_{DD}=V_{DDA}=3.3V, Regulator in run mode, LSI on, RTC on, All GPIOs analog mode	—	117.06	—	µA
		V_{DD}=V_{DDA}=3.3V, Regulator in low power under drive, LSI on, RTC on, All GPIOs analog mode	—	91.98	—	µA
	Supply current (Standby mode)	V_{DD}=V_{DDA}=3.3V, LSE off, LSI on, RTC on	—	7.83	—	µA
		V_{DD}=V_{DDA}=3.3V, LSE off, LSI on, RTC off	—	7.54	—	µA
		V_{DD}=V_{DDA}=3.3V, LSE off, LSI off, RTC off	—	6.85	—	µA
I_{BAT}	Battery supply current	V_{DD} not available, V_{BAT}=3.6 V, LSE on with external crystal, RTC on, Higher driving	—	1.74	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LSE on with external crystal, RTC on, Higher driving	—	1.59	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LSE on with external crystal, RTC on, Higher driving	—	1.38	—	µA
		V_{DD} not available, V_{BAT}=3.6 V, LSE on with external crystal, RTC on, Lower driving	—	1.07	—	µA
		V_{DD} not available, V_{BAT}=3.3 V, LSE on with external crystal, RTC on, Lower driving	—	0.92	—	µA
		V_{DD} not available, V_{BAT}=2.6 V, LSE on with external crystal, RTC on, Lower driving	—	0.72	—	µA

4.4 EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the following table, based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 11. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{ESD}	Voltage applied to all device pins to induce a functional disturbance	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-2	3B
V_{FTB}	Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V_{DD} and V_{SS} pins	VDD = 3.3 V, TA = +25 °C conforms to IEC 61000-4-4	4A

EMI (Electromagnetic Interference) emission testing result is given in the following table, compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 12. EMI characteristics

Symbol	Parameter	Conditions	Tested frequency band	Conditions		Unit
				48M	72M	
S_{EMI}	Peak level	VDD = 3.3 V, TA = +25 °C, compliant with IEC 61967-2	0.1 to 2 MHz	<0	<0	dBµV
			2 to 30 MHz	-3.7	-2.8	
			30 to 130 MHz	-6.5	-8	
			130 MHz to 1GHz	-7	-7	

4.5 Power supply supervisor characteristics

Table 13 Power supply supervisor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Power on reset threshold	—	2.30	2.40	2.48	V
V_{PDR}	Power down reset threshold		1.72	1.80	1.88	V
V_{HYST}	PDR hysteresis		—	0.6	—	V
$T_{RSTTEMP}$	Reset temporization		—	2	—	ms

4.6 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 14. ESD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=25 °C; JESD22-A114	—	—	7000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A=25 °C; JESD22-C101	—	—	2000	V

Table 15. Static latch-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LU	I-test	T_A=25 °C; JESD78	—	—	±200	mA
	V_{supply} over voltage		—	—	5.4	V

4.7 External clock characteristics

Table 16. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}	High speed external clock (HXTAL) frequency	V_{DD}=3.3V	4	8	32	MHz
C_{HXTAL}	Recommended load capacitance on OSC_IN and OSC_OUT	—	—	20	30	pF
D_{HXTAL}	HXTAL oscillator duty cycle	—	30	50	70	%
$I_{DDHXTAL}$	HXTAL oscillator operating current	V_{DD}=3.3V, T_A=25°C	—	1.0	—	mA
$t_{SUHXTAL}$	HXTAL oscillator startup time	V_{DD}=3.3V, T_A=25°C	—	2	—	ms

Table 17. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}	Low Speed External oscillator (LXTAL) frequency	V_{DD}=V_{BAT}=3.3V	—	32.768	—	KHz
C_{LXTAL}	Recommended load capacitance on OSC32_IN and OSC32_OUT	—	—	—	15	pF
D_{LXTAL}	LXTAL oscillator duty cycle	—	30	50	70	%
$I_{DDLXTAL}$	LXTAL oscillator operating current	Low Drive	—	0.7	—	µA
		High Drive	—	1.3	—	
$t_{SULXTAL}$	LXTAL oscillator startup time	V_{DD}=V_{BAT}=3.3V	—	2	—	s

4.8 Internal clock characteristics

Table 18. High speed internal clock (IRC8M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD}=3.3V	—	8	—	MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-4.0	—	+5.0	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-2.0	—	+2.0	%
		V_{DD}=3.3V, T_A=25°C	-1.0	—	+1.0	%
	IRC8M oscillator Frequency accuracy, User trimming step	—	—	0.5	—	%
D_{IRC8M}	IRC8M oscillator duty cycle	V_{DD}=3.3V, f_{IRC8M}=8MHz	45	50	55	%
$I_{DDIRC8M}$	IRC8M oscillator operating	V_{DD}=3.3V, f_{IRC8M}=8MHz	—	66	80	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	current					
$t_{SUIRC8M}$	IRC8M oscillator startup time	V_{DD}=3.3V, f_{IRC8M}=8MHz	—	1.8	2.5	us

Table 19. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD}=3.3V	—	48	—	MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD}=3.3V, T_A=-40°C ~+105°C	-4.0	—	+5.0	%
		V_{DD}=3.3V, T_A=0°C ~ +85°C	-3.0	—	+3.0	%
		V_{DD}=3.3V, T_A=25°C	-2.0	—	+2.0	%
	IRC48M oscillator Frequency accuracy, User trimming step	—	—	0.12	—	%
D_{IRC48M}	IRC48M oscillator duty cycle	V_{DD}=3.3V, f_{IRC48M}=16MHz	45	50	55	%
$I_{DDIRC48M}$	IRC48M oscillator operating current	V_{DD}=3.3V, f_{IRC48M}=16MHz	—	240	300	μA
$t_{SUIRC48M}$	IRC48M oscillator startup time	V_{DD}=3.3V, f_{IRC48M}=16MHz	—	2.5	4	us

Table 20. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}	Low Speed Internal oscillator (IRC32K) frequency	V_{DD}=V_{BAT}=3.3V, T_A=-40°C ~ +85°C	20	40	45	KHz
$I_{DDIRC32K}$	IRC32K oscillator operating current	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	0.4	0.6	μA
$t_{SUIRC32K}$	IRC32K oscillator startup time	V_{DD}=V_{BAT}=3.3V, T_A=25°C	—	110	130	μs

4.9 PLL characteristics

Table 21. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock frequency	—	1	—	25	MHz
f_{PLLOUT}	PLL output clock frequency	—	16	—	108	MHz
t_{LOCK}	PLL lock time	—	—	—	300	μs
I_{DD}	Current consumption on	VCO freq=108MHz	—	160	—	μA

	VDD					
I_{DDA}	Current consumption on VDDA	VCO freq=108MHz	—	300	—	μA
$Jitter_{PLL}$	Cycle to cycle Jitter	System clock	—	300	—	ps

4.10 Memory characteristics

Table 22. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A=-40°C ~ +85°C	100	—	—	kcycles
t_{RET}	Data retention time	T_A=125°C	20	—	—	years
t_{PROG}	Word programming time	T_A=-40°C ~ +85°C	200	—	400	us
t_{ERASE}	Page erase time	T_A=-40°C ~ +85°C	60	100	450	ms
t_{MERASE}	Mass erase time	T_A=-40°C ~ +85°C	3.2	—	9.6	s

4.11 GPIO characteristics

Table 23. I/O port characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Low level input voltage		V_{DD}=2.6V	—	—	1.03	V
			V_{DD}=3.3V	—	—	1.31	
			V_{DD}=3.6V	—	—	1.41	
	High Voltage tolerant IO Low level input voltage		V_{DD}=2.6V	—	—	1.02	V
			V_{DD}=3.3V	—	—	1.36	
			V_{DD}=3.6V	—	—	1.41	
V_{IH}	Standard IO High level input voltage		V_{DD}=2.6V	1.69	—	—	V
			V_{DD}=3.3V	1.99	—	—	
			V_{DD}=3.6V	2.11	—	—	
	High Voltage tolerant IO High level input voltage		V_{DD}=2.6V	1.68	—	—	V
			V_{DD}=3.3V	1.99	—	—	
			V_{DD}=3.6V	2.11	—	—	
V_{OL}	Low level output voltage		V_{DD}=2.6V, I_{IO}=8mA	—	—	0.21	V
			V_{DD}=3.3V, I_{IO}=8mA	—	—	0.19	
			V_{DD}=3.6V, I_{IO}=8mA	—	—	0.18	
			V_{DD}=2.6V, I_{IO}=20mA	—	—	0.54	
			V_{DD}=3.3V, I_{IO}=20mA	—	—	0.47	
			V_{DD}=3.6V, I_{IO}=20mA	—	—	0.45	
V_{OH}	High level output voltage		V_{DD}=2.6V, I_{IO}=8mA	2.40	—	—	V
			V_{DD}=3.3V, I_{IO}=8mA	3.10	—	—	
			V_{DD}=3.6V, I_{IO}=8mA	3.40	—	—	
			V_{DD}=2.6V, I_{IO}=20mA	1.95	—	—	
			V_{DD}=3.3V, I_{IO}=20mA	2.73	—	—	
			V_{DD}=3.6V, I_{IO}=20mA	3.07	—	—	
R_{PU}	Internal pull-up resistor	All pins	V_{IN}=V_{SS}	30	40	50	kΩ
		PA10	—	7.5	10	13.5	
R_{PD}	Internal pull-down resistor	All pins	V_{IN}=V_{DD}	30	40	50	kΩ
		PA10	—	7.5	10	13.5	

4.12 ADC characteristics

Table 24. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.6	3.3	3.6	V
V_{ADCIN}	ADC input voltage range	—	0	—	V_{REF+}	V
f_{ADC}	ADC clock	—	0.1	—	40	MHz
f_S	Sampling rate	12-bit	0.007	—	2.86	MSPS
		10-bit	0.008	—	3.33	
		8-bit	0.01	—	4.00	
		6-bit	0.012	—	5.00	
V_{IN}	Analog input voltage	16 external; 3 internal (including the battery voltage channel)	0	—	V_{DDA}	V
V_{REF+}	Positive Reference Voltage	—	—	V_{DDA}	—	V
V_{REF-}	Negative Reference Voltage	—	—	0	—	V
R_{AIN}	External input impedance	See ***Equation 2***	—	—	32.9	kΩ
R_{ADC}	Input sampling switch resistance	—	—	—	0.55	kΩ
C_{ADC}	Input sampling capacitance	No pin/pad capacitance included	—	—	5.5	pF
t_{CAL}	Calibration time	f_{ADC}=40MHz	—	3.275	—	μs
t_s	Sampling time	f_{ADC}=40MHz	0.0375	—	5.99	μs
t_{CONV}	Total conversion time (including sampling time)	12-bit	—	14	—	1/ f_{ADC}
		10-bit	—	12	—	
		8-bit	—	10	—	
		6-bit	—	8	—	
t_{SU}	Startup time	—	—	—	1	μs

Equation 2: R_{AIN} max formula $$R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 2) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

Table 25. ADC $R_{AIN\ max}$ for f_{ADC}=40MHz

T_s (cycles)	t_s (us)	$R_{AIN\ max}$ (KΩ)
1.5	0.0375	0.15
7.5	0.1875	2.96
13.5	0.3375	5.77
28.5	0.7125	12.8
41.5	1.0375	18.9
55.5	1.3875	25.4
71.5	1.7875	32.9
239.5	5.9875	N/A

Note: Guaranteed by design, not tested in production.

Table 26. ADC dynamic accuracy at f_{ADC} = 28 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=28MHz	10.5	10.6	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=2.6V	65	65.6	—	dB
SNR	Signal-to-noise ratio	Input Frequency=20KHz	65.5	66	—	
THD	Total harmonic distortion	Temperature=25℃	-74	-76	—	

Table 27. ADC dynamic accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=30MHz	10.7	10.8	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=3.3V	66.2	65.8	—	dB
SNR	Signal-to-noise ratio	Input Frequency=20KHz	66.8	67.4	—	
THD	Total harmonic distortion	Temperature=25℃	-71	-75	—	

Table 28. ADC dynamic accuracy at f_{ADC} = 36 MHz

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC}=36MHz	10.3	10.4	—	bits
SNDR	Signal-to-noise and distortion ratio	V_{DDA}=V_{REFP}=3.3V	63.8	64.4	—	dB
SNR	Signal-to-noise ratio	Input Frequency=20KHz	64.2	65	—	
THD	Total harmonic distortion	Temperature=25℃	-70	-72	—	

Table 29. ADC static accuracy at f_{ADC} = 14 MHz

Symbol	Parameter	Test conditions	Typ	Max	Unit
Offset	Offset error	f_{ADC}=14MHz V_{DDA}=V_{REFP}=3.3V	±2	±3	LSB
DNL	Differential linearity error		±0.9	±1.2	
INL	Integral linearity error		±1.1	±1.5	

4.13 DAC characteristics

Table 30. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.6	3.3	3.6	V
R_{LOAD}	Resistive load	Resistive load with buffer ON	5	—	—	kΩ
R_O	Impedance output	Impedance output with buffer OFF	—	—	15	kΩ
C_{LOAD}	Capacitive load	Capacitive load with buffer ON	—	—	50	pF
DAC_OUT_{min}	Lower DAC_OUT voltage	Lower DAC_OUT voltage with buffer ON	0.2	—	—	V
		Lower DAC_OUT voltage with buffer OFF	0.5	—	—	mV
DAC_OUT_{max}	Higher DAC_OUT voltage	Higher DAC_OUT voltage with buffer ON	—	—	V_{DDA}-0.2	V
		Higher DAC_OUT voltage with buffer OFF	—	—	V_{DDA}-1LSB	V
I_{DDA}	DC current consumption in quiescent mode with no load	Middle code on the input	—	—	500	μA
		Worst code on the input	—	—	560	
DNL	Differential non linearity	10-bit configuration	—	—	±0.5	LSB
		12-bit configuration	—	—	±2	
INL	Integral non linearity	10-bit configuration	—	—	±1	LSB
		12-bit configuration	—	—	±4	
Gain error	Gain error	—	—	±0.5	—	%
$T_{SETTLING}$	Settling time	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	0.3	0.5	μs
Update rate	Max frequency for a correct DAC_OUT change from code i to i±1LSB	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	—	4	MS/s
T_{WAKEUP}	Wakeup time from off state	C_{LOAD}≤50pF, R_{LOAD}≥5kΩ	—	1	2	μs
PSRR	Power supply rejection ratio	No R_{Load}, C_{LOAD}=50pF	—	-90	-75	dB

4.14 Comparators characteristics

Table 31. CMP characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.6	3.3	3.6	V
V_{IN}	Input voltage range	—	0	—	V_{DDA}	V
V_{BG}	Scaler input voltage	—	—	1.2	—	V
V_{SC}	Scaler offset voltage	—	—	±5	±10	mV
t_D	Propagation delay for 200mv step with 100mV overdrive	Ultra low power mode	—	0.93	—	μS
		Low power mode	—	0.47	—	μS
		Medium power mode	—	0.17	—	μS
		High speed power mode	—	37	—	nS
	Propagation delay for full range step with 100mV overdrive	Ultra low power mode	—	1.57	—	μS
		Low power mode	—	0.80	—	μS
		Medium power mode	—	0.21	—	μS
		High speed power mode	—	46	—	nS
I_{DD}	Current consumption	Ultra low power mode	—	1.53	—	μA
		Low power mode	—	2.84	—	
		Medium power mode	—	8.11	—	
		High speed power mode	—	66.1	—	
V_{offset}	Offset error	—	—	±12	—	mV
V_{hys}	No hysteresis	—	—	0	—	mV
	Low hysteresis	High speed power mode	—	10	—	
		All other power modes	—	10	—	
	Medium hysteresis	High speed power mode	—	18	—	
		All other power modes	—	18	—	
	High hysteresis	High speed power mode	—	36	—	
		All other power modes	—	36	—	

4.15 I2C characteristics

Table 32. I2C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	—	0	100	0	1000	KHz
$TSI_{L(H)}$	SCL clock high time	—	4.0	—	0.6	—	ns
$TSI_{L(L)}$	SCL clock low time	—	4.7	—	1.3	—	ns

4.16 SPI characteristics

Table 33. SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	30	MHz
$TSI_{K(H)}$	SCK clock high time	—	16	—	—	ns
$TSI_{K(L)}$	SCK clock low time	—	16	—	—	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	25	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	f_{PCLK}=54MHz	74	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	f_{PCLK}=54MHz	37	—	—	ns
$t_{A(SO)}$	Data output access time	f_{PCLK}=54MHz	0	—	55	ns
$t_{DIS(SO)}$	Data output disable time	—	3	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

4.17 USART characteristics

Table 34. USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	84	MHz
$TSI_{K(H)}$	SCK clock high time	—	5.5	—	—	ns
$TSI_{K(L)}$	SCK clock low time	—	5.5	—	—	ns

5 Package information

5.1 QFN package outline dimensions

Figure 8. QFN package outline

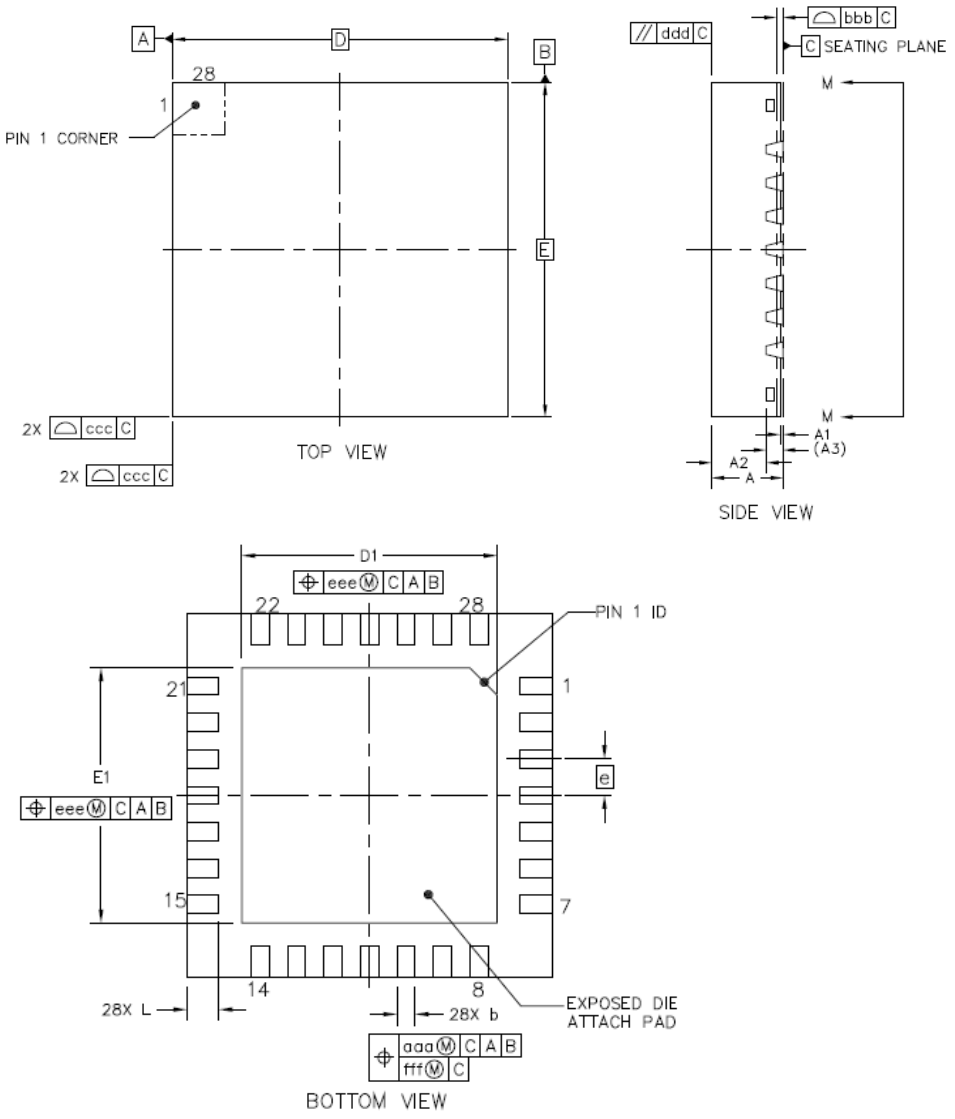


Table 35. QFN package dimensions

Symbol	QFN28		
	Min	Typ	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	-	0.65	0.67
A3	-	0.203	-
D	-	4.0	-
E	-	4.0	-
D1	2.7	2.8	2.9
E1	2.7	2.8	2.9
L	0.25	0.35	0.45
e	0.4		
b	0.15	0.2	0.25

Symbol	QFN32		
	Min	Typ	Max
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	-	0.65	0.67
A3	-	0.203	-
D	-	5.0	-
E	-	5.0	-
D1	3.4	3.5	3.6
E1	3.4	3.5	3.6
L	0.3	0.4	0.5
e	0.5		
b	0.2	0.25	0.3

(Original dimensions are in millimeters)

5.2 LQFP package outline dimensions

Figure 9. LQFP package outline

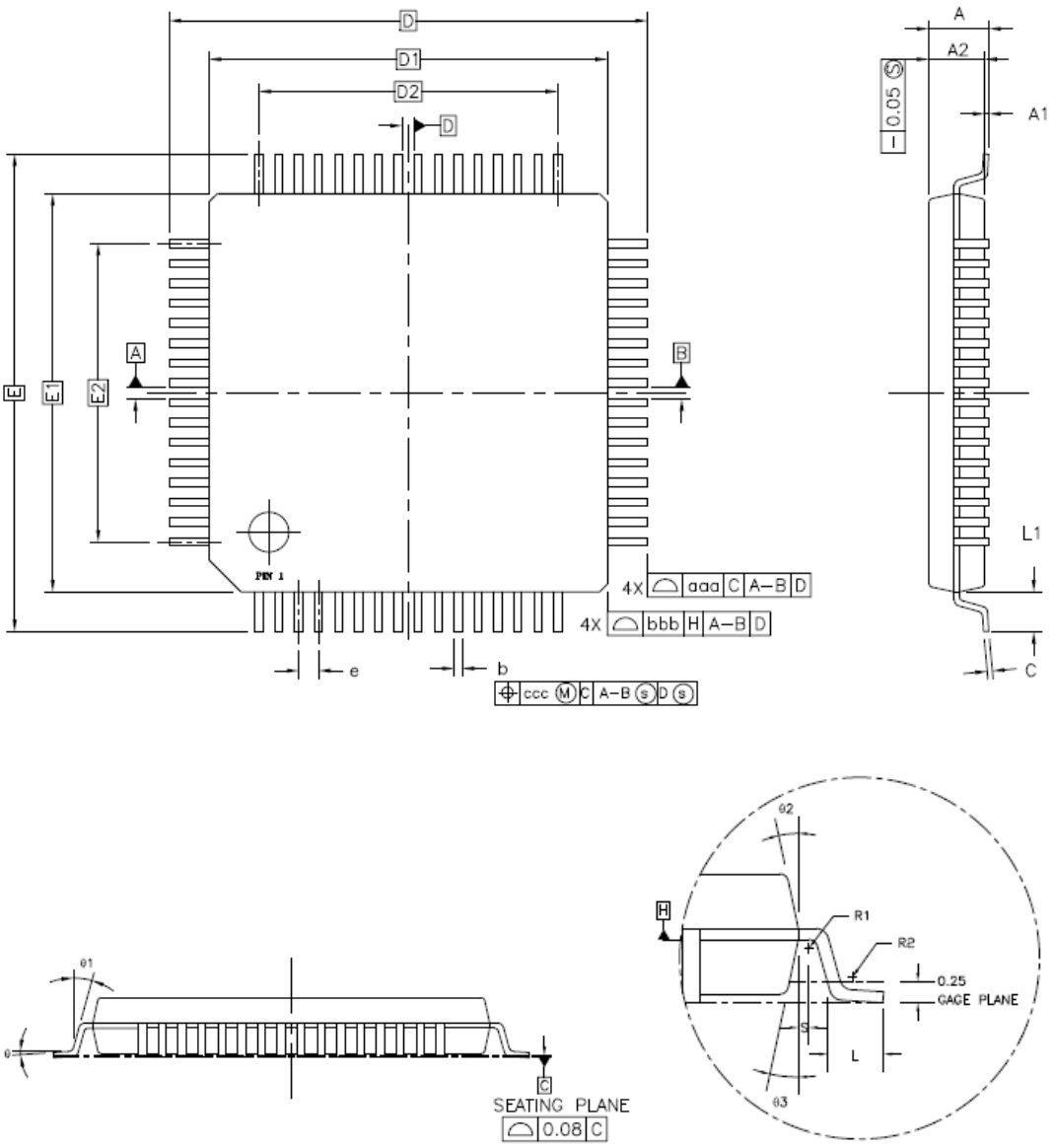


Table 36. LQFP package dimensions

Symbol	LQFP48		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
D	-	9.00	-
D1	-	7.00	-
E	-	9.00	-
E1	-	7.00	-
R1	0.08	-	-
R2	0.08	-	0.20
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	-	1.00	-
S	0.20	-	-
b	0.17	0.22	0.27
e	-	0.50	-
D2	-	5.50	-
E2	-	5.50	-
aaa	0.20		
bbb	0.20		
ccc	0.08		

Symbol	LQFP64		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D	-	12.00	-
D1	-	10.00	-
E	-	12.00	-
E1	-	10.00	-
R1	0.08	-	-
R2	0.08	-	0.20
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	-	1.00	-
S	0.20	-	-
b	0.17	0.20	0.27
e	-	0.50	-
D2	-	7.50	-
E2	-	7.50	-
aaa	0.20		
bbb	0.20		
ccc	0.08		

(Original dimensions are in millimeters)

6 Ordering Information

Table 37. Part ordering code for GD32F350xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32F350G4U6	16	QFN28	Green	Industrial -40°C to +85°C
GD32F350G6U6	32	QFN28	Green	Industrial -40°C to +85°C
GD32F350G8U6	64	QFN28	Green	Industrial -40°C to +85°C
GD32F350K4U6	16	QFN32	Green	Industrial -40°C to +85°C
GD32F350K6U6	32	QFN32	Green	Industrial -40°C to +85°C
GD32F350K8U6	64	QFN32	Green	Industrial -40°C to +85°C
GD32F350C4T6	16	LQFP48	Green	Industrial -40°C to +85°C
GD32F350C6T6	32	LQFP48	Green	Industrial -40°C to +85°C
GD32F350C8T6	64	LQFP48	Green	Industrial -40°C to +85°C
GD32F350CBT6	128	LQFP48	Green	Industrial -40°C to +85°C
GD32F350R4T6	16	LQFP64	Green	Industrial -40°C to +85°C
GD32F350R6T6	32	LQFP64	Green	Industrial -40°C to +85°C
GD32F350R8T6	64	LQFP64	Green	Industrial -40°C to +85°C
GD32F350RBT6	128	LQFP64	Green	Industrial -40°C to +85°C

7 Revision History

Table 38. Revision history

Revision No.	Description	Date
1.0	Initial Release	Jun.6, 2017
1.1	Characteristics values updated in ***Table 10. Power consumption characteristics***	Jun.20, 2017